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D. Remarks

Claim Objections:

Claims 1, 2, 4, 9, and 15, 16, 18, 19, and 20 were amended to address these objections.

Claims 1, 2, and 4 were amended to include first clock enable signal and chip enable signal outputs from the data processing circuit ending control of the semiconductor memory device and second clock enable signal and chip enable signal outputs from the different processing circuit starting control of the semiconductor memory.

Claim 9 was amended to include "another" in front of the data processing circuit in line 14.

Claims 15, 16, 18, 19, and 20 were amended to include "first" and "second" processing circuits and "first" and "second" control outputs to clarify the claim.

Rejection of Claims 1, 3, 5, 9, 10, and 14-17 Under 35 U.S.C. §103(a), based on Applicant's Background Art (BACKGROUND ART) in view of *Wilcox et al.* (USP 6,510,099).

The rejection of claims 1, 3, and 5 will first be addressed.

Claim 1 has been amended to clarify an element of the invention.

The invention of amended claim 1 is directed to a data processing apparatus that arbitrates sharing of a single semiconductor memory circuit among multiple data processing circuits. The data processing apparatus includes a semiconductor memory circuit and a data processing circuit supplies the semiconductor memory circuit with a first clock enable signal output to the clock enable signal input and a first chip select signal output to the chip select signal input. In the data processing apparatus, before the data processing circuit ends control of the semiconductor memory circuit and stops supplying the first clock enable signal output and first chip select signal input, a different data processing circuit starting control of the semiconductor memory circuit supplies the semiconductor memory circuit with a second clock enable signal output and a second chip enable signal output to the clock enable signal input and chip select signal input. The second clock enable signal output and second chip enable signal output having clock enable signal and chip select signal logic values at the same state as those provided by the data processing circuit ending control of the semiconductor memory circuit.

As is well understood, to establish a prima facie case of obviousness, a rejection must meet three basic criteria. First, there must be some suggestion or motivation to modify a

reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference(s) must teach or suggest all claim limitations.[1]

The rejection admits that the BACKGROUND ART does not disclose "before the data processing circuit ends control of the semiconductor memory circuit and stops supplying the first clock enable signal output and first chip select signal output, a different data processing circuit starting control of the semiconductor memory circuit supplies the semiconductor memory with a second clock enable signal output to the clock enable signal input and a second chip enable signal output to the chip enable signal input, the second clock enable signal output and the second chip enable output having clock enable signal and chip select signal logic values at the same state as the first clock enable signal output and first chip enable signal output provided by the data processing circuit ending control of the semiconductor memory circuit", as recited in amended claim 1.[2]

However, the other reference relied upon by the rejection, *Wilcox et al.*, does not show such a limitation, either.

Wilcox et al. shows a single memory controller (106) providing control lines (324) to a plurality of memory devices in a memory system (110).[3] *Wilcox et al.* also shows that the control lines (324) include first and second chip select signal (CS_1 and CS_2) and first and second clock enable signals (CKE_1 and CKE_2). Signals CS_1 and CKE_1 go to one row of DDR SDRAM memory devices and CKE_2 go to a second row of DDR SDRAM devices (i.e. going to separate chip select inputs and separate clock select inputs in the memory devices.

Also, *Wilcox* shows only one controller sharing a number of memory devices and providing signals to a memory bus (114). That is, there is no other device (i.e., controller, data processing circuit) that "starts control" of any memory device from the memory controller (106). All other devices (i.e. processor 102, graphic controller 120, and I/O controller 108) are connected to the memory controller (106) and not to the memory system (110), therefore, the memory controller must always maintain control over the memory system (110).

This is illustrated in the below figure of the reference:

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[1] MPEP §2143.
[2] See page 4, first paragraph of Office Action dated 07/20/2006.
[3] See FIG. 3 of *Wilcox et al.* showing a memory controller (106) providing control lines (324) to memory system (110).

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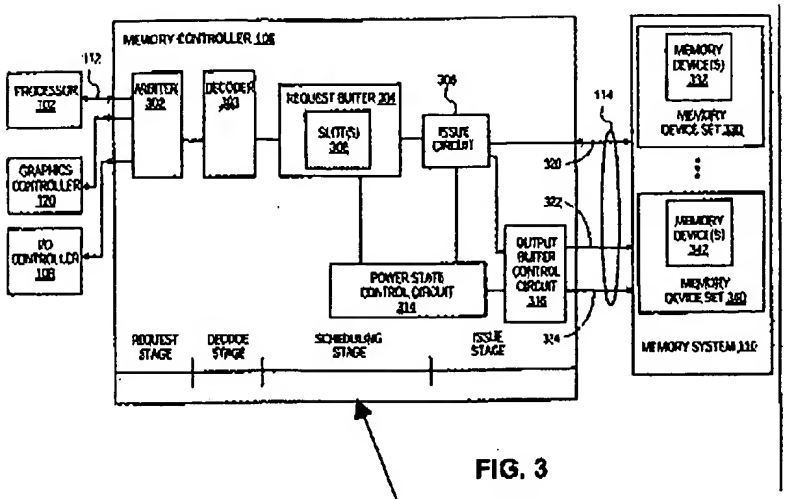

FIG. 3

See FIG. 3 of *Wilcox et al.* above, memory controller 106 is the only element connected to memory system (110) and therefore must always maintain control over memory system (110). Nowhere is it shown "a different data processing circuit starting control of a semiconductor memory circuit and supplying the semiconductor memory circuit with the clock enable and chip enable signal ... before the data processing circuit ends control of the semiconductor memory".

For these reasons, *Wilcox et al.* is not believed to show "a different data processing circuit starting control of a semiconductor memory circuit and supplying the semiconductor memory circuit with a second clock enable signal output to the clock enable signal input and a second chip enable signal output to the chip enable signal input, the second clock enable signal output and the second chip enable signal output" "before the data processing circuit ends control of the semiconductor memory" according to the claimed signal activations, as recited in amended claim 1.

Further, because both references appear silent as to such control switching operations of a clock enable signal and chip select signal from one data processing circuit to another data processing circuit, the cited combination of references is not believed to be suggestive of such a limitation, either.

For all of these reasons, the combination of references is not believed to show or suggest all the limitations of amended claim 1, and this ground for rejection are traversed.

The rejection of claims 9, 10, and 14 will now be addressed.

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The data processing apparatus of amended claim 9 includes a semiconductor memory circuit that is controlled by control signal inputs to at least one control input. At least one control line is coupled to the at least one control input of the semiconductor memory circuit. A plurality of data processing circuits that share access to the semiconductor memory circuit, each data processing circuit having a control output coupled to the at least one control line. When one data processing circuit ends control of the semiconductor memory circuit, the data processing circuit provides a control signal at the control output at a predetermined potential for a first time period before ending the control signal. Subsequently, when another data processing circuit starts control of the semiconductor memory circuit, the another data processing circuit provides a control signal at its control output at the predetermined potential within the first time period.

To address this rejection, the arguments set forth with regard to claim 1 are incorporated herein by reference. Namely, neither reference shows or suggests "another data processing circuit" taking control over a semiconductor memory circuit from a first data processing circuit according to the control signal potentials and time periods, as recited in claim 9. In particular, *Wilcox et al.* shows a memory controller (106) always maintaining control over a memory system (110).

Claim14, which depends from claim 9, is believed to be separately patentable over the cited reference. Claim 14 recites that "at least one control line is directly connected to the control input of the semiconductor memory circuit and the control output of each of the plurality of data processing circuits".

The rejection relies on the BACKGROUND ART to show the limitations of claim 14. Applicant does not believe such teachings are shown or suggested. Applicant's FIG. 4 of the BACKGROUND ART shows two controllers 102 (i.e., data processing circuits) that provide signals via signal lines (106) and data buses (105). However, no signal lines (106) of one controller are directly connected to the outputs of multiple data processing circuits. Instead, such signals lines (106) are commonly provided to arbiter (103). Similarly, no bus lines (105) of one controller are directly connected to the outputs of multiple controllers. Instead, data buses (105) are commonly provided to bus control circuit (104).

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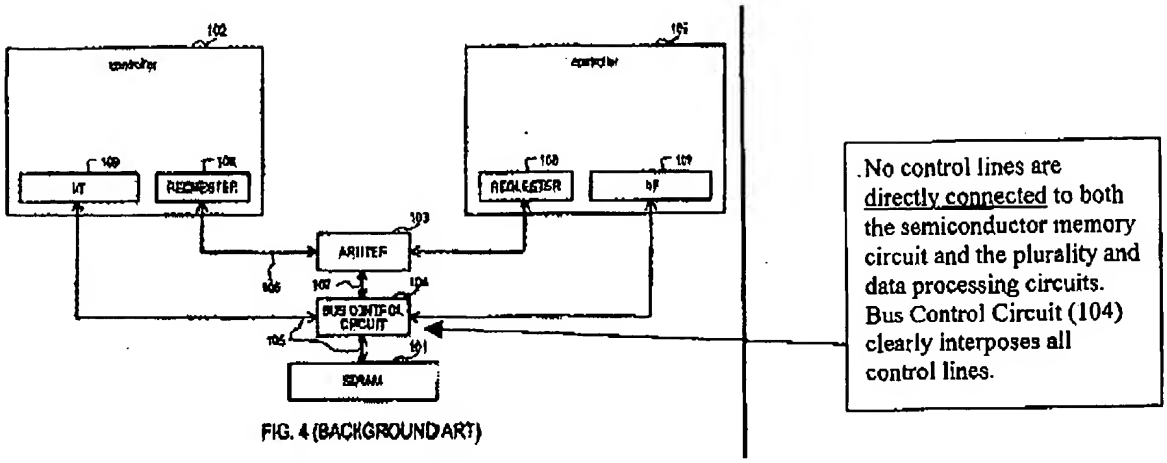

FIG. 4 (BACKGROUND ART)

Because the BACKGROUND ART only teaches connection to an interposing circuit, the reference is not believed to shows or suggests a direct connection, as recited in claim 14, either.

For these reasons, the combination of references is not believed to show or suggest all the limitations of claim 14, and this ground for rejection is traversed.

The rejection of claims 15–17 will now be addressed.

The invention of amended claim 15 is directed to a method of sharing a semiconductor memory circuit with a plurality of data processing circuits. The method includes, when a first data processing circuit ends control of the semiconductor memory circuit, driving first control outputs connected to control lines for the semiconductor memory circuit to predetermined logic values, and subsequently placing the first control outputs in a high impedance state. The method also includes, when a second data processing circuit starts control of the semiconductor memory circuit, second driving control outputs connected to the control lines to the predetermined logic values prior to the first control outputs of the first data processing circuit that is ending control of the semiconductor memory circuit being placed in the high impedance state.

To address this rejection, the arguments set forth with regard to claim 1 are incorporated herein by reference. Namely, neither reference shows or suggests "when a different one of the plurality of data processing circuits starts control of the semiconductor memory circuit, driving control outputs prior to the control outputs of the data processing circuit that is ending control of the semiconductor memory circuit". Rather, the teachings relied upon to show the limitations of claim teach only a single controller controlling multiple memory devices.

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To further address this rejection, the arguments set forth with regard to claim 14 are incorporated herein by reference. Namely, neither reference shows or suggests the control lines connected to both the first data processing circuit that ends control of the semiconductor memory circuit and the second data processing circuit that starts control of the semiconductor memory circuit. Both references show intervening circuits between the control lines.

Accordingly, because the cited combination of references is not believed to show or suggest all of the Applicant's claim limitations, this ground for rejection is traversed.

Rejection of Claims 4, 7, 11 and 18-20 Under 35 U.S.C. §103, based on Applicant's Background Art in view of *Wilcox et al.*, and further in view of *Askinazi et al.* (USP 4,453,21).

The rejection of claims 4 and 7 will first be addressed.

To the extent that this ground for rejection relies on the combination of the BACKGROUND ART in view of *Wilcox et al.*, Applicant incorporates by reference herein the same general comments set forth above for independent claim 1.

The rejection of claim 11 will now be addressed.

To the extent that this ground for rejection relies on the combination of the BACKGROUND ART in view of *Wilcox et al.*, Applicant incorporates by reference herein the same general comments set forth above for independent claim 9.

The rejection of claim 18-20 will now be addressed.

To the extent that this ground for rejection relies on the combination of the BACKGROUND ART in view of *Wilcox et al.*, Applicant incorporates by reference herein the comments set forth above for independent claim 15.

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Claims 1, 2, 4, 9, 15, 16, 18, 19, and 20 have been amended not in response to the cited art, but to clarify elements of the invention. No new matter has been added. The present claims 1-20 are believed to be in allowable form. It is respectfully requested that the application be forwarded for allowance and issue.

Respectfully Submitted,

October 19, 2006

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